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MOS Transistor and Method of Manufacture

Cross-Reference To Related Application

This application claims priority of Provisional Application Serial No. 60/168,036 which was filed November 30, 1999 and Provisional Application Serial No. 5 60/140,999 which was filed on June 24, 1999.

Field of the Invention

The present invention relates integrated circuits generally, and particularly to a MOS transistor and its method of manufacture.

Background of the Invention

10 As integrated circuit (IC) complexity increases, the size of devices within the IC must decrease. To decrease the size of a device, the various elements (features) of a device must be reduced proportionately. This is known as device scaling. One common device in integrated circuits is the metal oxide semiconductor field effect transistor (MOSFET). In a MOSFET, device scaling requires a reduction gate and
15 channel lengths. As gate and channel lengths are reduced, a number of effects can result in unacceptable reliability and performance in the MOSFET. These effects are commonly referred to as short-channel effects and are particularly problematic in devices having channel lengths of approximately 1.25 μm or less.

20 One effect of the reduced channel length devices is increased horizontal and vertical electric field components, particularly in the drain region. This increase in the electric field can cause inversion-layer carriers to be accelerated (or become "hot") to an extent that they may cause a number of harmful device phenomena, commonly referred to as hot carrier effects. Ultimately, these phenomena can adversely impact device reliability and performance.

25 One way to overcome hot carrier effects is through the use of a lightly doped drain (LDD) structure. In an LDD structure, the source and drain have graded doping profiles. In the source and drain regions nearest the channel, the doping level is

lower, relative to the more highly doped source and drain regions farther from the channel. The lightly doped source and drain regions serve to reduce the electric field strength in the regions of the channel near the source and drain. This reduced electric field strength has been somewhat successful in reducing hot carrier generation, and thereby hot carrier effects.

While the LDD structure has been useful in reducing short channel effects such as hot carrier effects, there are certain drawbacks to its use. One such drawback is an increase in series resistance between the source and the drain (referred to as series source-drain resistance (R_{sd})). This is due to the reduced doping level at the lightly doped source and drain region. This increased resistance results in a reduction in the saturation current (also referred to as drive current I_{dsat} or "on" current I_{on}). A reduction in I_{on} may result in a reduction in device switching speed. A MOSFET being used as a switch may be thought of as a device for charging and discharging a capacitor. The time required to charge the capacitor is directly related to the current. As such, if the current is reduced, the switching speed is reduced. Accordingly, this increase in R_{sd} in conventional devices incorporating an LDD is undesirable.

Another drawback to the LDD structure is the complexity of its fabrication. In order to fabricate this structure, there are many additional processing steps that must be added to the process flow in MOSFET fabrication. These include additional photolithographic masking levels, LDD implantation and the formation of a dielectric spacer.

Accordingly, what is needed is a device that overcomes the above illustrated drawbacks of LDD MOSFET devices.

Summary of the Invention

The present invention relates to a reduced feature size MOS transistor that has improved short channel effects but does not include an LDD structure. In an illustrative embodiment, a MOS transistor has a gate length of 1.25 μm or less. Moreover, by eliminating the use of the LDD structure, series source-drain resistance is reduced resulting in improved drive current and switching speed.

In another embodiment, a technique for fabricating a MOS transistor is disclosed. Illustratively, a gate structure having a length of 1.25 μm or less is formed over a substrate. Thereafter, a source and a drain are formed without lightly doped regions.

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Brief Description of the Drawings

The invention is best understood from the following detailed description when read with the accompanying drawing figures. It is emphasized that the various features are not necessarily drawn to scale. In fact, dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

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Figure 1 is a cross-sectional view of an exemplary embodiment of the present invention.

Figures 2-4 are cross-sectional views of an illustrative fabrication sequence according to an exemplary embodiment of the present invention.

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Figure 5 is a graphical representation of time versus substrate current indicative of hot carrier aging (HCA) according to an exemplary embodiment of the present invention and for a conventional device.

Figure 6 is a graphical representation of drive gate length versus drive current for conventional devices which use an LDD structure and for exemplary devices of the present invention.

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Detailed Description

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The present invention will now be described more fully with reference to the accompanying drawing figures, in which exemplary embodiments of the present invention are shown. Referring to Fig. 1, a MOS transistor 10 in accordance with an exemplary embodiment of the present invention is first described. Illustratively, the transistor 10 includes a gate structure 11 disposed over a substrate 12. A channel 13 is disposed between a source 14 and a drain 15. The gate structure 11 includes an oxide layer 16, which includes a first oxide portion 17 and a second oxide portion 18. The

second oxide portion 18 forms an interface 19 with the substrate 12. The oxide layer may have a layer of material 20 disposed between it and a conductive layer 21.

For purposes of illustration, the transistor 10 is an NMOS device. As such, the source 14 and drain 15 are doped n^+ , while the substrate is p-type. Of course, the present invention may be used in other devices including PMOS and complementary MOS (CMOS) devices. The substrate 12 is illustratively silicon; it may be monocrystalline or polycrystalline silicon. Most generally it is oxidizable silicon. Layer 20 may be a high-k material, including but not limited to tantalum pentoxide, barium-strontium titanate, and silicate dielectric materials. Additionally, other materials may be disposed between the conductive layer 21 and the oxide layer 16 to achieve a variety of results as would be appreciated by the artisan of ordinary skill.

The MOS field effect transistor of the exemplary embodiment of Figure 1, does not incorporate a lightly doped drain or a lightly doped source. This is in clear contrast to conventional devices having gate lengths of approximately $1.25\ \mu\text{m}$ or less which employ an LDD structure to mitigate hot carrier effects. In the exemplary embodiment shown in Fig. 1 the device 10 may have a gate length (and thus a channel length), L , on the order of approximately $1.25\ \mu\text{m}$ or less. Moreover, sub-micron devices may incorporate the present invention. It is anticipated that the gate lengths may be in the range of approximately $0.25\ \mu\text{m}$ to approximately $0.05\ \mu\text{m}$. Finally, as is well known in the art, device scaling mandates that the gate length and other device features must be proportional according to scaling rules. Thus, the oxide layer 16 has a thickness that is scaled to the gate length chosen. Accordingly, in the illustrative embodiment, gate lengths in the range of approximately $1.25\ \mu\text{m}$ to approximately $0.05\ \mu\text{m}$ corresponds to the oxide layer 11 having a thickness in the range of approximately $20.0\ \text{nm}$ to approximately $1.5\ \text{nm}$, respectively.

The oxide/substrate interface 19 is substantially stress-free and planar. Moreover, oxide layer 16 has a reduced number of interface traps (N_{it}) and a reduced defect density (D_o) compared to conventional oxides. These and other characteristics of the oxide layer 16 are useful in achieving the invention of the present disclosure. Further details of the oxide and its characteristics may be found in U.S. Patent Application (Attorney Docket No. Chen 2-18-74-93), entitled "High Quality Oxide For Use In Integrated Circuits", the disclosure of which is specifically incorporated by reference.

herein. (This patent application is assigned to the assignee of the present invention, and is filed on even date herewith).

As discussed in more detail below, the device of the present invention has certain advantageous characteristics over conventional devices. These characteristics include an improvement in drive current and switching speed. Moreover, this increase in drive current may be realized even though the channel may require an increased doping level used to curb an undesired short channel effect known as punch-through (discussed more fully herein). Additionally, the effects of hot carriers, which can result in a degradation in device reliability, can be minimized in devices using the present invention. Finally, the present invention is advantageous because it reduces the complexity of fabrication. To this end, the relatively complex processing sequences needed to form LDD structures, which are considered a necessary trade-off in conventional short channel length devices, are unnecessary in the present invention.

Turning now to Figs.2-4, an illustrative fabrication sequence is described. Figure 2 is the oxide growth sequence used in the formation of oxide layer 16 over the substrate 13, resulting the formation of a substantially stress free and planar interface 19. The details of this fabrication sequence may be found in U.S. Patent Application (Attorney Docket No. Chen 4-17-133-157), entitled "A Process For Fabricating Oxides", the disclosure of which is specifically incorporated herein by reference. (This patent application is assigned to the assignee of the present invention, and is filed on even date herewith). Thereafter, as shown in Fig. 3, the gate structure-11 is completed via conventional processing schemes which may include: deposition of a high-k layer; amorphous silicon or polycrystalline silicon deposition, gate implantation and gate masking steps.

As shown in Fig. 3, after the gate structure 11 is completed, the channel 13 is formed. This may be carried out by standard implantation techniques. The channel doping is raised via tilted "halo" or "pocket" implants 30 of the same conductivity type as the channel. For the exemplary NMOS device, an implant such as boron in the energy range of 5-40keV, a dose in the range of approximately 5×10^{11} to approximately 5×10^{13} /cm², at an implant tilt angle in the range of 7-45° (with respect to a normal to the substrate) may be used. Similarly, for a PMOS device a phosphorus implant in the energy range of 20-120keV, a dose in the range of approximately 5×10^{11} to approximately 5×10^{13}

/cm², at an implant tilt angle in the range of 7-45° may be used. The illustrative channel doping concentration is now in the range of approximately 1×10^{16} to approximately 1×10^{19} /cm³. This channel doping step serves to reduce punchthrough and thus short channel effects in the devices.

5 As shown in Fig. 4, after the halo implantation, the source 14 and drain 15 are formed. In the exemplary NMOS device, this is carried out by implanting arsenic in the energy range of 5-50keV, a dose in the range of approximately 5×10^{14} - to approximately 5×10^{15} /cm², and an implant tilt angle in the range of 0-7°. Similarly, for the PMOS device the source and drain is formed via a boron implant in the energy range
10 of 0.5-10keV, a dose in the range of approximately 5×10^{14} - to approximately 5×10^{15} /cm², and a implant tilt angle in the range of 0-7°. Alternatively, a BF₂ implant in the energy range of 5-50keV, a dose range of approximately 5×10^{14} - to approximately 5×10^{15} /cm², and a implant tilt angle in the range of 0-7°. The resulting doping levels in the source and drain are in in the range of approximately 1×10^{20} /cm³ to approximately 5×10^{20} /cm³.
15 In clear contrast to the prior art LDD devices, the source 14 and drain 15 in the illustrative embodiment of Figs. 1 and 4 are substantially uniformly doped, and do not include a lightly doped region.

 Through a review of Figs. 2-4, the relative ease of fabrication of the illustrative embodiment may be appreciated. The process needed to fabricate
20 conventional short channel devices includes the fabrication of an LDD. At minimum, this adds a mask formation step so that a first implantation could be carried out. This is needed to form the lightly doped source and drain regions. Thereafter, a spacer must be deposited and etched. In conventional LDD devices, the spacer is needed in the fabrication of the more heavily doped regions of the source and drain. In addition to
25 adding to the complexity of fabrication, the added implants and spacer may have deleterious effects on the resultant device. These include, for example increased series source/drain resistance, R_{sd} , and thus reduced saturated drive current I_{dsat} and switching speed.

 As mentioned previously, hot carrier effects can adversely impact device
30 reliability. In MOS transistors having gate lengths of approximately 1.25 microns or less, hot carrier effects result from increased horizontal and vertical components of the electric field in the reduced length channel. This causes inversion-layer charges to be accelerated

(or heated) to an extent that they may cause a number of harmful device phenomena, commonly referred to as hot carrier effects. Hot carrier effects can ultimately degrade the reliability of the device. This is commonly referred to as hot carrier aging (HCA).

Hot carrier aging is believed to be due to interface trap generation or the breaking of passivated dangling bonds by hot carriers. Dangling bonds in the silicon-silicon dioxide interface are conventionally passivated in a hydrogen ambient, thereby reducing the number of interface traps. While this passivation technique has met with some success in conventional devices, hot carriers can readily break silicon-hydrogen bonds, thereby re-establishing the previously passivated interface traps. The traps in the interface act as scattering centers, thereby reducing the mobility of carriers within the channel.

As is known, the drive current, I_{on} (or saturation current, I_{dsat}), and the transconductance, g_m are directly proportional to the mobility of the carriers in the channel. Accordingly, as the scattering centers become more abundant due to hot carrier effects, the mobility of carriers in the channel is reduced, and the drive current and transconductance are reduced. Thus, the number of interface traps can cause the device to degrade (age) due to drift in device parameters such as drive current and transconductance. This degradation has a deleterious impact on device reliability.

The oxide layer 16 has a reduced incidence of dangling silicon bonds, and thereby a reduced number of interface traps. Applicants theorize that this is a result of a more complete oxidation process and because the interface is substantially stress-free and planar. Moreover, since there are fewer interface traps in the oxide of the present invention, there are fewer traps to be passivated with hydrogen. It is anticipated that there will be less device drift due to hydrogen release in devices which incorporate the oxide of the present invention. Finally, while the LDD structure has helped to reduce hot carrier effects in short channel devices, the illustrative embodiment of the present invention results in a greater reduction in hot carrier effects

The resulting improvement in hot carrier aging can be seen clearly in the graphical representation of Fig. 5. The hot carrier aging criteria by convention is a 15% change in transconductance. The plot labeled 51 is for a device according to an illustrative embodiment of the present invention incorporating a $0.24 \mu m$ gate length

with an oxide layer having a thickness of 5 nm (50Å). The plot labeled 50 is for a conventional device having the same gate length, which incorporates an LDD structure to reduce the ill-effects of hot carriers. As is evident from Fig. 5, the substrate current limit of $1 \mu\text{A}/\mu\text{m}$ is achieved at 100 hours in a conventional LDD MOSFET; and in an
5 exemplary device of the present invention this is limit achieved at 400 hours. As will be readily appreciated to those of ordinary skill in the art, in devices having comparable gate lengths, hot carrier aging is improved by a factor of four by the present invention when compared to conventional devices, which require the LDD structure.

In addition to improvements in reliability through reduced HCA, the
10 device of the present invention also has increased drive current as a result of both increased carrier mobility and reduced source-drain resistance. The increased mobility is a result of the reduction in scattering centers, as discussed above. The reduction in R_{sd} is a direct benefit of the elimination of the lightly doped source and drain regions used in conventional LDD structures. To this end, because the incidence of hot carriers is
15 reduced by means other than the LDD structure, it is not needed in the exemplary device of the present invention. Accordingly, the source and drain doping levels of the present invention are substantially uniform being in the range of approximately 1×10^{20} to approximately $5 \times 10^{20}/\text{cm}^3$. This results in a source-drain sheet resistance in the range of approximately 50 to approximately 150 ohms/sq. This translates directly into R_{sd} of
20 approximately 25 to approximately 100 ohms per μm of gate width in an exemplary device of the present invention. (It is of interest to note that by convention, gate width is measured along the z-direction in the coordinate axis shown in Fig.1). In contrast, the lightly doped regions of a conventional lightly doped source and lightly doped drain are on the order of 1×10^{19} to $5 \times 10^{19}/\text{cm}^3$. The corresponding source/drain sheet resistance of
25 a conventional LDD is in the range 500-1500 ohms/sq. This results in R_{sd} of 100-200 ohms per μm of gate width in such conventional devices.

As a result of the reduction in the series source drain resistance by virtue of the present invention, the drive current is improved. Turning to Figure 6, a graphical representation of gate length versus drive current is shown. Plot 60 is a graph of the drive
30 current of exemplary devices of the present invention. Plot 61 is for conventional devices which use an LDD structure. Clearly, an improvement in transistor drive current, I_{dsat} , is measured in illustrative devices of the present invention when compared to conventional device having similar feature sizes, and which incorporate an LDD structure.

As alluded to above, the increased drive current results in a faster switching speed. Again, a MOSFET being used as a switch may be thought of as a device that charges and discharges a capacitor. These capacitors are intrinsic parts of CMOS circuits arising from such elements as MOS gate capacitance, source/drain junction capacitance, and metal interconnect capacitance. The time required to charge the capacitor is directly related to the current. As such, if the drive current is increased, the switching speed is increased. Having improved drive current levels results in a ring oscillator circuit using exemplary MOSFETs of the present invention having switching speeds on the order of 25% greater than conventional LDD MOS transistors

Moreover, this increase in the drive current in the exemplary device of the present invention is realized even though the threshold voltage V_t may be slightly increased. To this end, one phenomena that may occur in reduced channel length devices is known as punch-through. Punch through is normally observed when the applied gate voltage is well below V_t . Punch-through occurs when the drain depletion region widens when the reverse bias on the drain is increased. When this depletion region width is great enough, the source and drain depletion regions may meet and an unacceptable level of carrier flow may occur. This results in poor charge control, and is manifest in unacceptable off current levels. While the LDD structure, having reduced doping levels at the source and drain regions nearest the channel may reduce the effects of punch through, often this must be mitigated by increasing the doping level of the channel to reduce the drain/source depletion region width. However, the increased channel doping concentration can increase the threshold voltage as a greater voltage is required to create inversion for conduction in the channel. The increased threshold voltage may cause a reduction in the drive current. Thus, the trade-off to the reduction in punch through via increased channel doping is often a reduction in drive current in conventional LDD devices.

Applicants have found that the exemplary device of the present invention maintains an increase in the drive current in spite of the increase in threshold voltage. Illustratively, in a 0.24 μm feature size device, the drive current increased 20% over a similar conventional LDD device having similar device feature sizes. This was in spite of a 50 mV increase in the threshold voltage. Applicants attribute this to the reduction in the series source-drain resistance realized through the invention of the present disclosure.

The invention having been described in detail, it is clear that various modification and variations of the embodiments disclosed above may be readily apparent to one having ordinary skill in the art having had the benefit of the present disclosure. To the extent that these modifications and variations include the invention, a transistor that
5 mitigates short channel effects without the use of an LDD structure, such are deemed within the scope of the present invention.